

Bitec

DSP Solutions for Industry & Research

***HSMC Quad Video Mosaic Reference
Design***

Version 0.1



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Revision history

Version	Comment
V0.1	Beta release

Introduction

This reference design demonstrates the use of the Bitec Hsmc Quad Video for mosaic on a 1080P Full HD video signal. The four composite/s-video channels are combined with a Full HD 1080P internally generated test pattern to produce a 1080P, mosaic output video stream. The design exploits enhancements new to version 8.1 of the Altera VIP to achieve the much higher DDR2 bandwidth required by the design.

A block diagram of the SoPC is shown in Figure 1. Both the input video signals are triple frame buffered to allow synchronization to the output video stream driven by the local 134Mhz pixel clock.

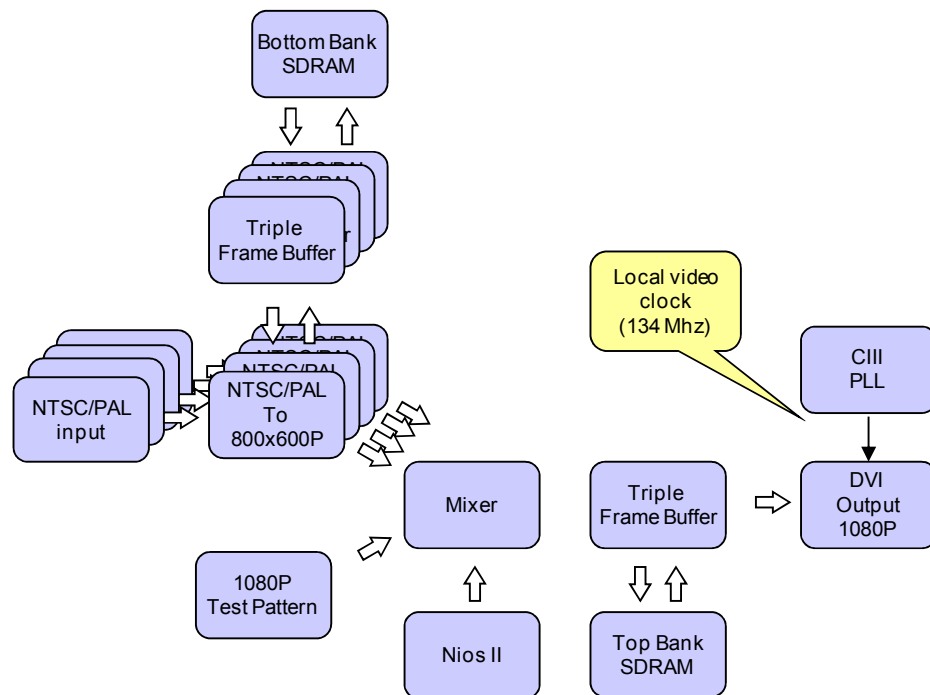


Figure 1 Picture-in-picture block diagram

Detail of the conversion between NTSC/PAL to 800x600P is shown in Figure 2. The input signal is first converted from YCrCb to RGB. The resulting RGB interlaced image stream is then converted to a progressive image stream through

the de-interlace component. The progressive image stream is then scaled to 800x600 before triple buffering.

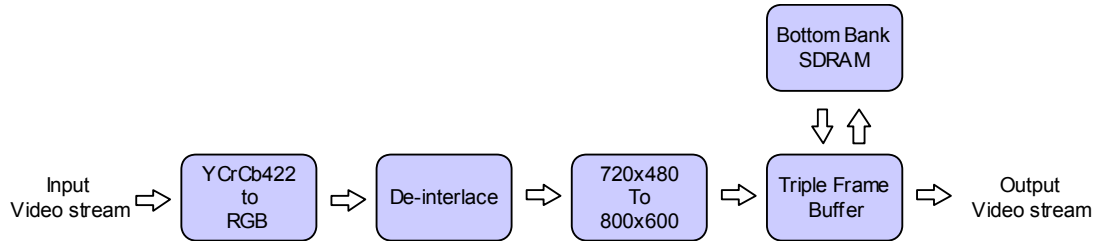


Figure 2 NTSC/PAL to 800x600P video pipeline block diagram

The mixer component is responsible for combining the five image streams. This component has a Nios II control port to allow run time changes to the mixer behaviour. In this reference design the PiP sub-pictures coordinates are continuously changed by the Nios II thus moving the PiP around the background 1080P video in real-time.

New to version 8.1 VIP is the ability to clock the Avalon master interfaces at different clock rates. This is exploited in this reference design as can be seen in the SoPC diagram. The dual clock core features in the v8.1 VIP enable far higher bandwidth designs to be achieved more easily.

Both the top and bottom DDR2 memory banks are used to achieve the necessary bandwidth. The top bank is used to buffer the 4-NTSC signals and the bottom bank is used to buffer the 1080P input video signal.

Installation

The hardware configuration is shown in Figure 3. A 1080P video source and composite video source are required. A PC DVI or HDMI video signal can be used for the demo. The composite signal can be any NTSC/PAL video signal.

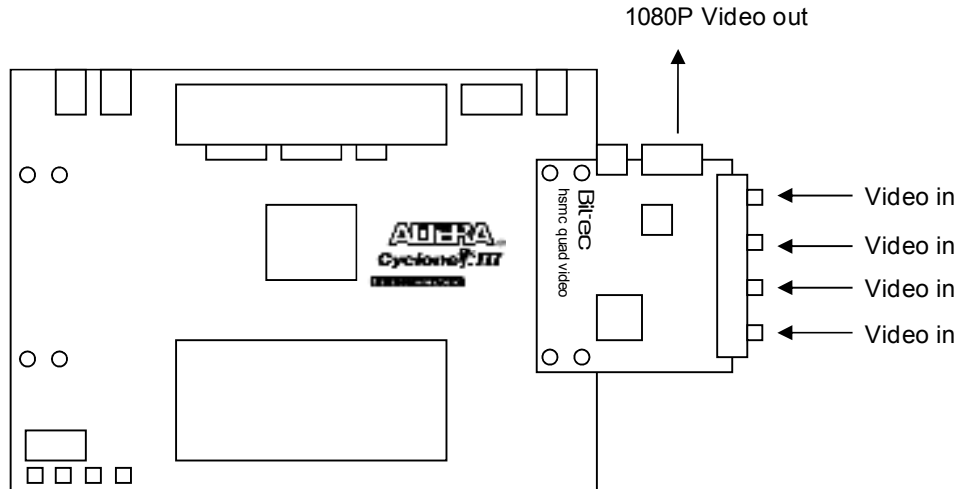


Figure 3 Hardware configuration

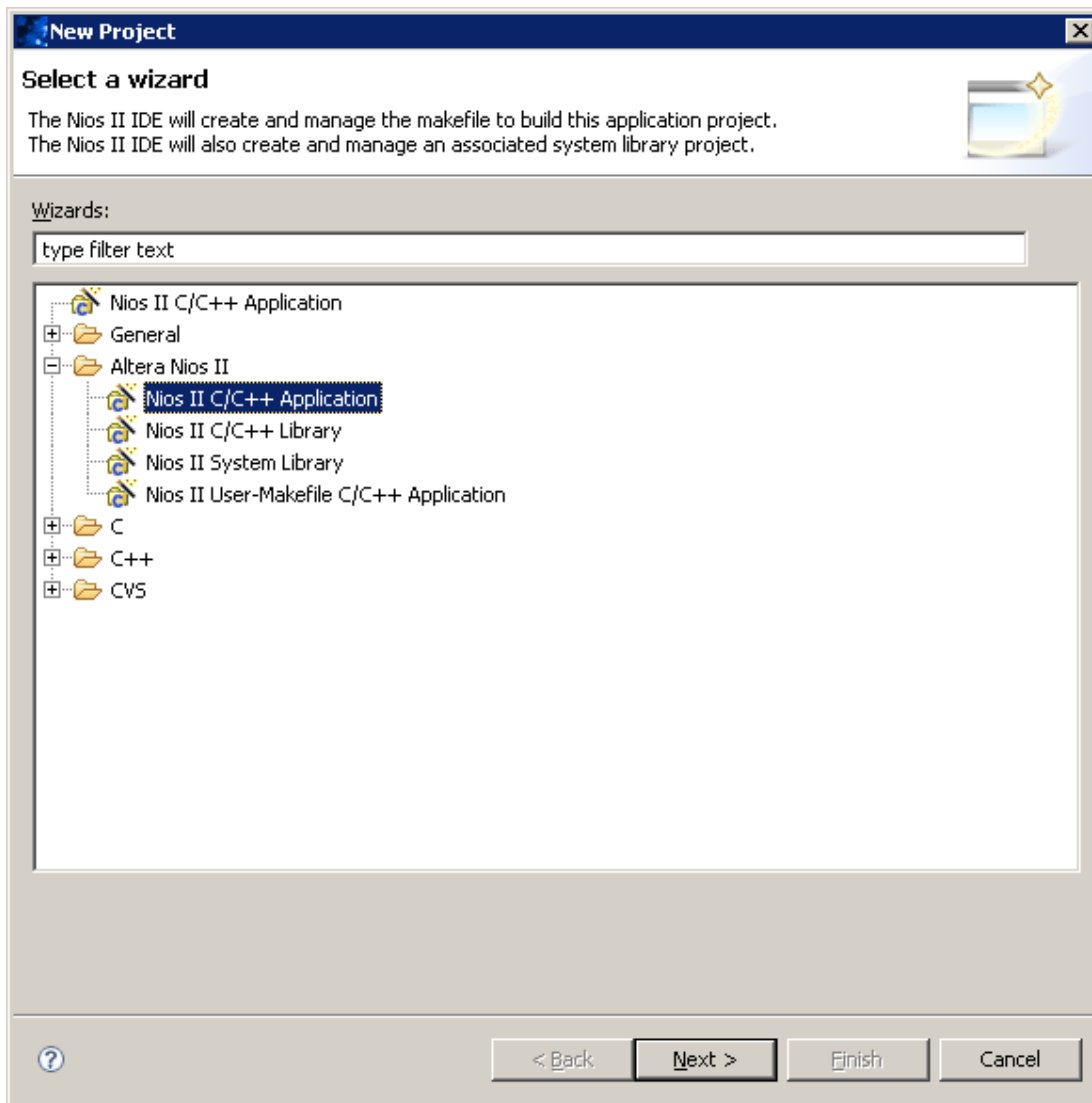
The demo Nios II software executes from onchip memory and will run when the FPGA SOF file is downloaded. The steps necessary to re-build the software are detailed below.

Building the demo software

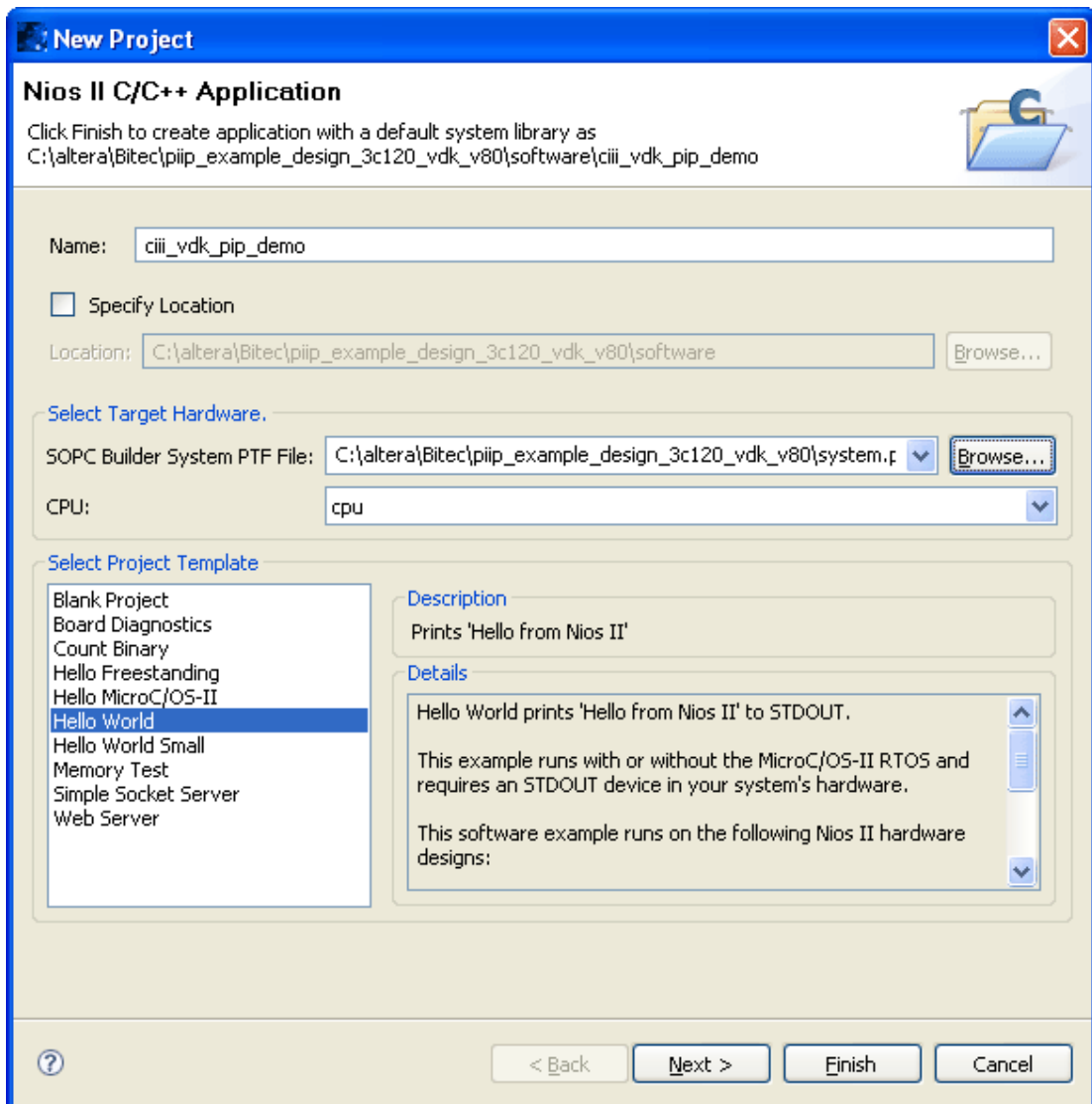
Before executing the demo software it is first necessary to create a Nios II project and include the supplied source files.

Open the Nios II IDE and “Switch Workspace” to the “Software” directory.

Create a new “Nios II C/C++ Application” from the File->New menu.



Change the project name to `ciii_vdk_pip_demo` and choose the SOPC Builder System PTF to select the `system.ptf` demo Nios II processor description file.



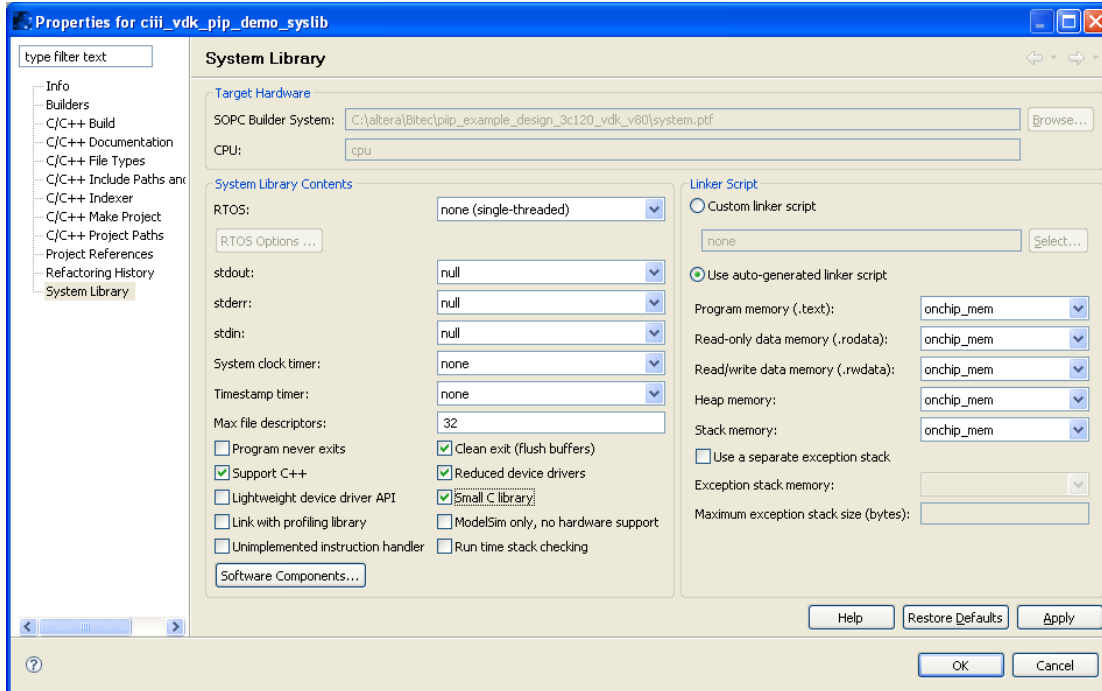
Click “Next” and then “Finish”. Two directories will be created below the Software directory.

Copy the supplied source files into the newly created “cii_vdk_pip_demo” directory.

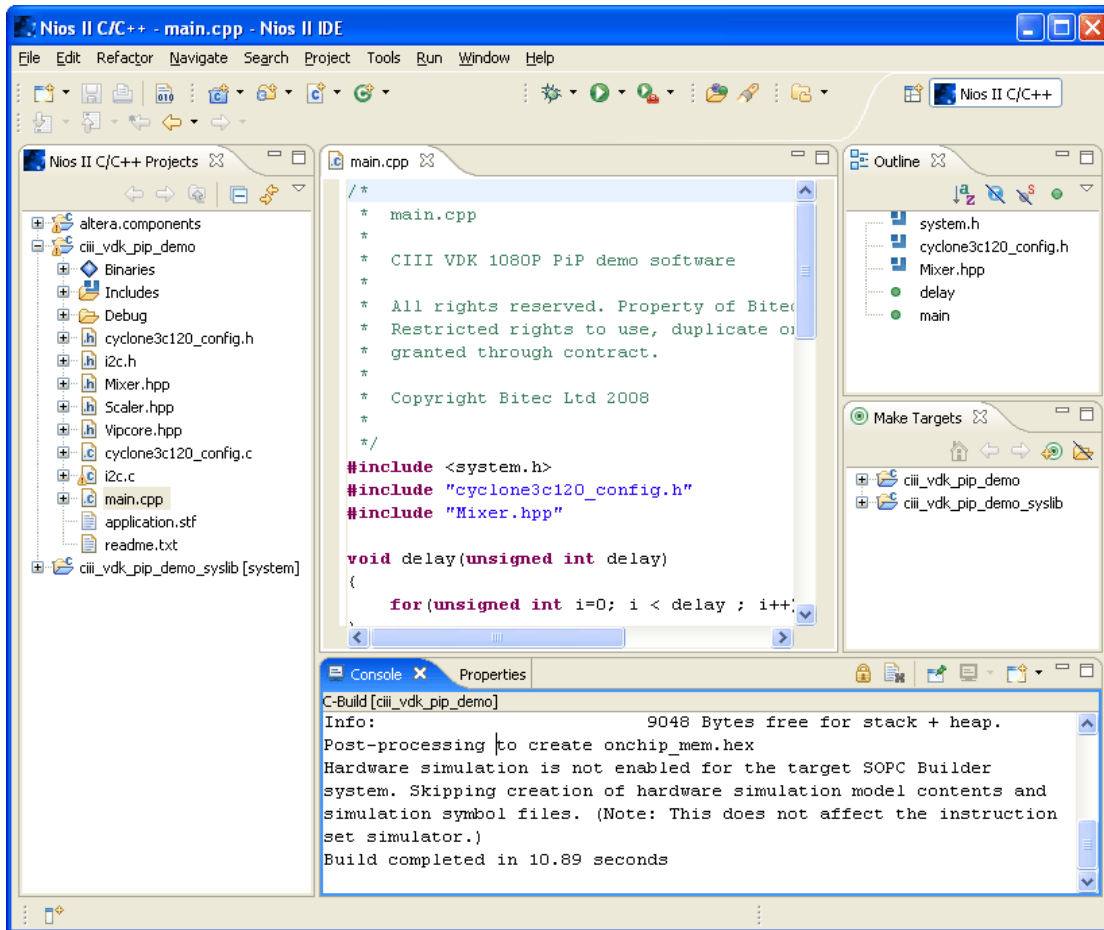
Highlight the cii_vdk_pip_demo directory in “Project Browser” pane “Refresh” using F5 or File->Refresh.

Select the auto generated hello_world.c and delete.

Before building, set the memory options to “onchip_mem” in the system library properties. Also select the “Reduced Drivers” and “Small C Library” options.



The project is now ready for build and debug.



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